



DIGITAL AUDIO INTERFACE RECEIVER

FEATURES

- Standard Digital Audio Interface Receiver (EIAJ1201)
- Sampling Rate: 32 / 44.1 / 48 / 88.2 / 96 kHz
- Recover 128 / 256 / 384 / 512 f_s System Clock
- Very Low Jitter System Clock Output (75 ps Typically)
- On-Chip Master Clock Oscillator, Only an External Crystal Is Required:
24.576 / 22.5792 / 18.432 / 16.9344 / 16.384 / 12.288 / 11.2896 / 8.192 / 6.144 / 5.6448 / 4.096 MHz Crystals Are Available
- Selectable Output PCM Audio Data Format
- Selectable Crystal Clock and PPL Clock Operation Mode
- Output User Bit Data, Flag Signals, and Channel Status Data With Block Start Signal
- Single 3.3-V Power Supply
- Package: 28 SSOP

APPLICATIONS

- AV Receiver
- MD Player
- DAC Unit

DESCRIPTION

The DIR1703 is a digital audio interface receiver (DIR) which receives and decodes audio data up to 96 kHz according to the AES/EBU, IEC958, S/PDIF, and EIAJCP340/1201 consumer and professional format interface standards. The DIR1703 demultiplexes the channel status bit and user bit directly to serial output pins, and has dedicated output pins for the most important channel status bits. It also includes extensive errors reporting.

The significant advantages of the DIR1703 are *96-kHz sampling rate capability* and *Low-jitter clock recovery by the Sampling Period Adaptive Controlled Tracking (SpAct™) system*. The input signal is reclocked with the patented *Sampling period Adaptive controlled tracking system* for maximum quality. These features are required for recent consumer and professional audio instruments, in which the DIR has an interface to any kind of delta-sigma type ADC/DAC with a 96-kHz sampling rate.



This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

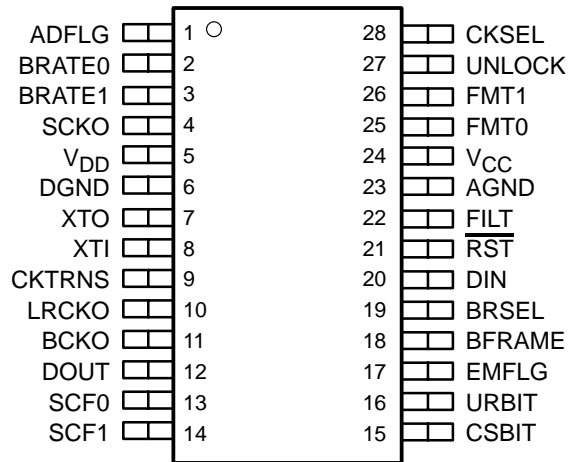


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DIR1703
(TOP VIEW)



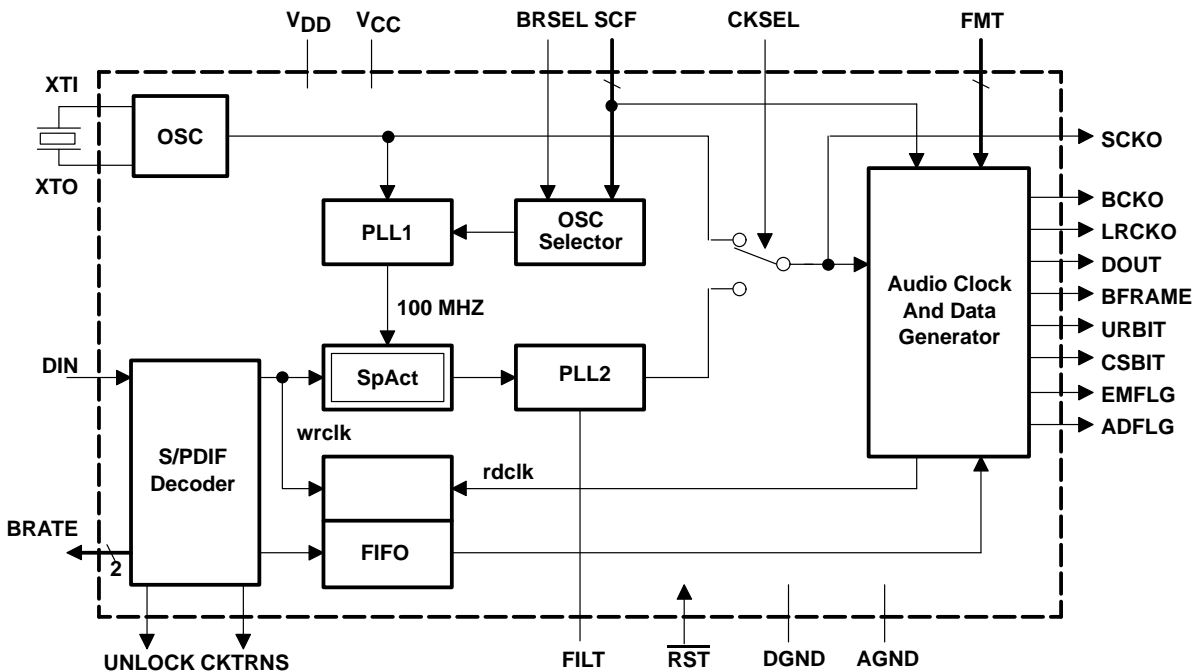
PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	OPERATION TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER†	TRANSPORT MEDIA
DIR1703E	SSOP–28	324†	–25°C to +85°C	DIR1703E	DIR1703E	Rails
					DIR1703E/2K	Tape and Reel

† TI equivalent no. 4040065.

‡ Models with a slash (/) are available only in tape and reel in the quantities indicated (e.g., /2K indicates 2000 devices per reel). Ordering 2000 pieces of DIR1703E/2K will get a single 2000-piece tape and reel.

block diagram



Terminal Functions

TERMINAL NAME	PIN	I/O	DESCRIPTIONS
ADFLG	1	O	Audio data or digital data flag
BRATE0	2	O	f_S rate flag 0 (32 k, 44.1 k, 48 k, and 88 k / 96 k)
BRATE1	3	O	f_S rate flag 1 (32 k, 44.1 k, 48 k, and 88 k / 96 k)
SCKO	4	O	System clock output
VDD	5	–	Digital power supply, +3.3 V
DGND	6	–	Digital ground
XTO	7	O	Crystal oscillator output
XTI	8	I	Crystal oscillator input, external clock input
CKTRNS	9	O	Clock transition status output
LRCKO	10	O	Audio latch enable (LRCK, f_S) output
BCKO	11	O	Audio bit clock output
DOUT	12	O	Audio serial data output
SCF0	13	I	System clock frequency select (128/256/384/512 f_S) (see Note 1)
SCF1	14	I	System clock frequency select (128/256/384/512 f_S) (see Note 1)
CSBIT	15	O	Channel status bit output (see Note 2)
URBIT	16	O	User bit output (see Note 2)
EMFLG	17	O	Emphasis flag
BFRAME	18	O	Block start clock (B-frame)
BRSEL	19	I	Default bit rate select (32 / 44.1 / 48 / 88.2 / 96 kHz) (see Note 1)
DIN	20	I	S/PDIF data digital input (see Note 4)
$\overline{\text{RST}}$	21	I	Reset input, active LOW (see Note 3)
FILT	22	–	External filter
AGND	23	–	Analog ground
VCC	24	–	Analog power supply, 3.3V
FMT0	25	I	Audio data format select (see Note 1)
FMT1	26	I	Audio data format select (see Note 1)
UNLOCK	27	O	PLL unlock or parity error flag
CKSEL	28	I	System clock operation mode selected. Low: PLL, High: Crystal (see Note 1)

- NOTES: 1. Schmitt trigger input with internal pulldown (TYP 51 k Ω), 5 V tolerant.
2. Serial outputs are utilized for both consumer and professional application.
3. Schmitt trigger input with internal pullup (TYP 51 k Ω), 5 V tolerant.
4. CMOS level input with internal pulldown (TYP 51 k Ω), 5 V tolerant.

electrical characteristics, all specifications at $T_A = 25^\circ\text{C}$, $V_{CC} = V_{DD} = 3.3\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
DIGITAL INPUT/OUTPUT							
$V_{IH}^{(5)}$	Input logic level		2		5.5	VDC	
$V_{IL}^{(5)}$					0.8		
$V_{IH2}^{(6)}$			$70\%V_{DD}$				
$V_{IL2}^{(6)}$					$30\%V_{DD}$		
$V_{IH3}^{(7)}$			$70\%V_{DD}$				5.5
$V_{IL3}^{(7)}$					$30\%V_{DD}$		
$V_{OH}^{(8)}$	Output logic level	$I_O = 1\text{ mA}$	$V_{DD}-0.4$			VDC	
$V_{OL}^{(8)}$		$I_O = -2\text{ mA}$			0.5		
$V_{OH}^{(9)}$		$I_O = 2\text{ mA}$	$V_{DD}-0.4$				
$V_{OL}^{(9)}$		$I_O = -4\text{ mA}$					0.5
$I_{IH}^{(10)}$	Input leakage current	$V_{IN} = V_{DD}$		65	100	μA	
$I_{IL}^{(10)}$		$V_{IN} = 0\text{ V}$	-10		10		
$I_{IH}^{(11)}$		$V_{IN} = V_{DD}$	-10		10		
$I_{IL}^{(11)}$		$V_{IN} = 0\text{ V}$	-100	-65			
$I_{IH}^{(6)}$		$V_{IN} = V_{DD}$	-10		10		
$I_{IL}^{(6)}$		$V_{IN} = 0\text{ V}$	-10		10		
$f_S^{(12)}$	Input sampling frequency		32		96	kHz	
SCKO	System clock frequency		4.096	128/256/ 384/512 f_S	49.152	MHz	
t_j	SCKO clock jitter			75		ps RMS	
	SCKO duty cycle			50%			
	XTI clock accuracy		-500	See Table 3	500	ppm	
S/PDIF INPUT							
	Duty cycle	$V_{IN} = 1.5\text{ V}$, $f_S = 96\text{ kHz}$	15%		85%		
	Jitter	$V_{IN} = 1.5\text{ V}$			± 10	ns p-p	
POWER SUPPLY REQUIREMENTS							
V_{DD} , V_{CC}	Voltage range		3	3.3	3.6	VDC	
$I_{CC}(V_{CC})$	Supply current (see Note 13)			3.4	4.7	mA	
$I_{DD}(V_{DD})$				26	36		
P_D	Power dissipation			100		mW	
TEMPERATURE RANGE							
	Operation temperature		-25		85	$^\circ\text{C}$	
θ_{JA}	Thermal resistance	28-pin SSOP		100		$^\circ\text{C/W}$	

- NOTES: 5. TTL compatible, except pins 8, 20: XTI, DIN.
6. Pin 8: XTI (CMOS logic level).
7. Pin 20: DIN (CMOS logic level).
8. Pins 1–3, 9, 17–18, 27: ADFLG, BRATE0, BRATE1, CKTRNS, EMFLG, BFRAME, UNLOCK.
9. Pins 4, 10–12, 15–16: SCKO, LRCKO, BCKO, DOUT, CSBIT, URBIT.
10. Pins 13–14, 19–20, 25–26, 28: SCF0, SCF1, BRSEL, DIN, FMT0, FMT1, CKSEL.
11. Pin 21: RST
12. f_S is defined as the incoming audio sampling frequency per channel.
13. No load connected to SCKO, LRCKO, BCKO, DOUT, CSBIT, URBIT. Power supply current varies according to the system clock frequency.

basic operation theory

The DIR1703 is operated as either a PLL clock operation mode or a crystal clock operation mode. These basic operation modes are user selectable.

Sampling period adaptive controlled tracking system (SpAct) is a newly developed clock recover architecture, giving very low jitter clock from S/PDIF data input.

The DIR1703 has two PLLs, PLL1 and PLL2. SpAct is supplied with a 100 MHz executing clock from PLL1.

The DIR1703 requires system clock input for operation of SpAct at both the PLL clock operation mode and the crystal clock operation mode. This system clock can be obtained by connecting a crystal resonator at the XTI/XTO pins or applying an external clock input at the XTI pin as shown in Figure 1.

PLL2 generates the system clock SCKO by using the output signal of the SpAct. The source of SCKO, either OSC (crystal) or PLL2, is selected by the CKSEL pin (called PLL clock operation mode and crystal clock operation mode).

In the PLL clock operation mode, when the S/PDIF signal goes to noninput, SCKO may hold the latest tracked frequency.

Also, the DIR1703 indicates the unlocked state by a high level output at the UNLOCK pin. When the S/PDIF signal restarts, the analog PLL will lock to the incoming S/PDIF signal with very low jitter. The PLL lock-in time is around 1 ms using the SpAct.

Then, the DIR1703 indicates the locked status by a low output at the UNLOCK pin. In this status, the BRATE pins simultaneously indicate the bit rate of the incoming S/PDIF signal.

After \overline{RST} (pin 21) is removed, SCKO is set to the default frequency, which can be selected by the BRSEL and SCF pins. The sampling rate (f_S), 32 k, 44.1 k, 48 k, 88.2 k, or 96 k is selected by the BRSEL pin. The system clock frequency, 128, 256, 384, or 512 f_S is also selected by the SCF pins.

In the crystal clock operation mode, the crystal oscillator generates three audio clocks SCKO, BCKO, and LRCKO. In this mode, DOUT is always set to mute (zero). BRATE and UNLOCK can be indicated according to the incoming S/PDIF signal.

If CKSEL (pin 28) is connected to UNLOCK (pin 27), which indicates the S/PDIF decoding status and the PLL2 lock-state, the system clock source can be selected automatically when the S/PDIF signal is active and the bit rate is detected.

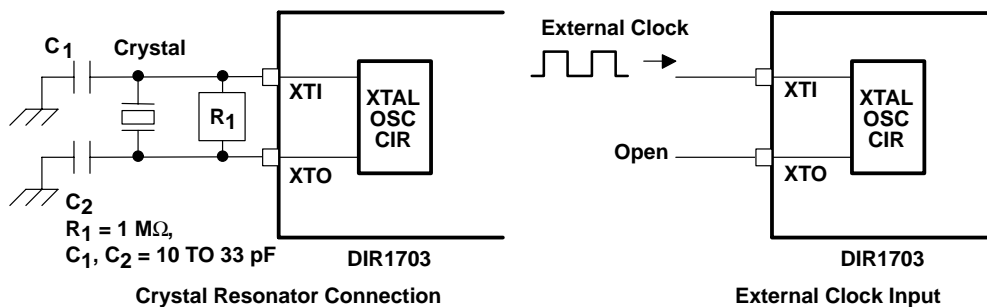


Figure 1. System Clock Connections

system clock output

The primary function of the DIR1703 is to recover audio data and a low jitter clock from a digital audio transmission line. The system clock (SCKO) can be selected in two clocks that are generated by the crystal oscillator clock (crystal mode) or the PLL clock (PLL mode) by the SpAct.

The two operation modes are selected by the CKSEL pin. In the PLL clock operation mode, the clock that can be generated is SCKO ($128 / 256 / 384 / 512 f_S$, shown in Table 1), BCKO ($64 f_S$), and LRCKO ($1 f_S$). SCKO is the output of the voltage controlled oscillator (VCO) in an analog PLL. The PLL function consists of a VCO, phase and frequency detector, and an external second-order loop filter. The closed-loop transfer function, which specifies the PLL jitter attenuation characteristics, is shown in Figure 2. In the crystal clock operation mode, SCKO can be generated from several crystal oscillators shown in Table 2.

The crystal frequency should be defined for internal PLL by connecting the BRSEL pin to one of the output pins BFRAME, EMFLG, URBIT, or CSBIT as shown in Table 3. A 12.288 MHz crystal resonator can be used for 96-kHz – $128 f_S$ (CSBIT), 48-kHz – $256 f_S$ (OPEN) and 32-kHz – $384 f_S$ (BFRAME). If BRSEL is not connected to any pins, the 48-kHz sampling rate is selected. The system clock frequency of both modes can be selected by control data at SCF0 and SCF1 pins shown in Table 4.

Table 5 shows the state of the system and the condition of audio clocks and flags in both the PLL and crystal operation modes. In the crystal clock operation mode, SpAct also detects the bit rate of the incoming S/PDIF signal and indicates the state at the UNLOCK pin. Therefore, by connecting CKSEL pin 28) to UNLOCK (pin 27), the system clock source can be selected automatically when the S/PDIF signal arrives and the bit rate is detected. The required accuracy for clock frequency of the crystal resonator or external clock input is ± 500 ppm.

Table 1. Generated System Clock (SCKO) PLL Clock Operation Mode

SAMPLING RATE	128 f_S	256 f_S	384 f_S	512 f_S
32 kHz	yes	yes	yes	yes
44.1 kHz	yes	yes	yes	yes
48 kHz	yes	yes	yes	yes
88.2 kHz	yes	yes	yes	yes
96 kHz	yes	yes	yes	yes

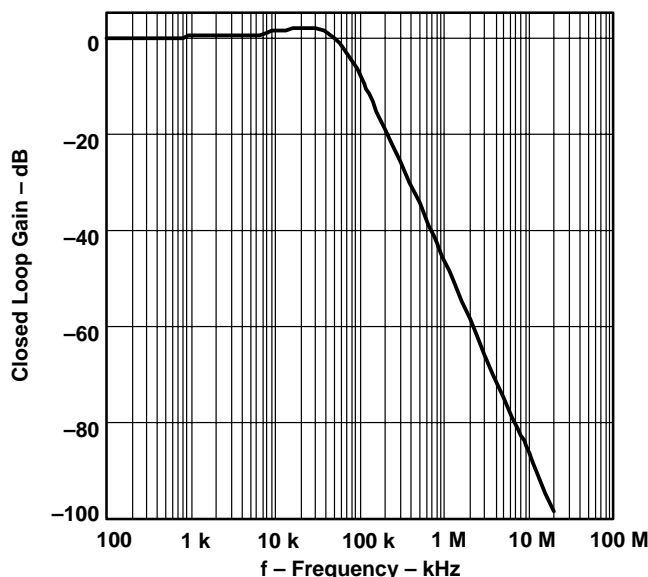


Figure 2. Jitter Attenuator Characteristics With Specified Loop Filter

system clock output (continued)

Table 2. Generated System Clock (SCKO) Crystal Clock Operation Mode

SAMPLING RATE	128 f _S	256 f _S	384 f _S	512 f _S
32 kHz	yes	yes	yes	yes
44.1 kHz	yes	yes	yes	yes
48 kHz	yes	yes	yes	yes
88.2 kHz	yes	yes	yes	yes
96 kHz	yes	yes	See Note 14	See Note 14

NOTE 14: External clock only

Table 3. Selectable Crystal Oscillator

SAMPLING RATE	128 f _S	256 f _S	384 f _S	512 f _S	BRSEL CONNECTED TO
32 kHz	4.096 MHz	8.192 MHz	12.288 MHz	16.384 MHz	BFRAME
44.1 kHz	5.6448 MHz	11.2896 MHz	16.9344 MHz	22.5792 MHz	EMFLG
48 kHz	6.144 MHz	12.288 MHz	18.432 MHz	24.576 MHz	open
88.2kHz	11.2896 MHz	22.5792 MHz	33.8688 MHz (see Note 14)	45.1584 MHz (see Note 14)	URBIT
96 kHz	12.288 MHz	24.576 MHz	36.864 MHz (see Note 14)	49.152 MHz (see Note 14)	CSBIT

Table 4. System Clock Selection

SCF1	SCF0	SYSTEM CLOCK
LOW	LOW	128 f _S
LOW	HIGH	256 f _S
HIGH	LOW	384 f _S
HIGH	HIGH	512 f _S

system clock output (continued)

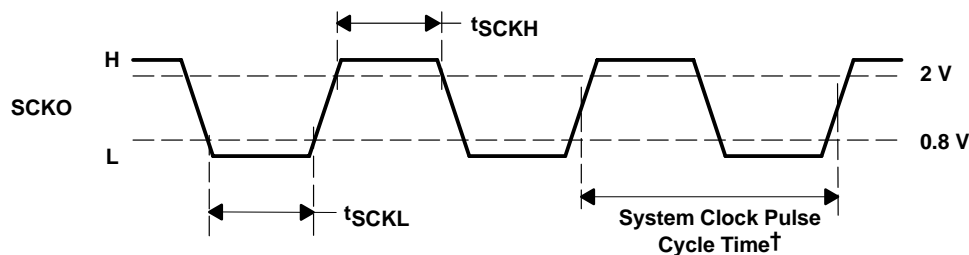
Table 5. System Clock Operation Mode

MODE	CONDITIONS		CLOCK AND DATA OUTPUTS							
	CKSEL	S/PDIF DATA	SCKO	BCKO	LRCKO	DOUT	BRATE	UNLOCK	CS. UR BIT	AD. EMFLG
PLL	LOW	After RESET	Default PLL [†] (128, 256, 384, 512 f _S)	Default PLL [†] (64 f _S)	Default PLL [†] (1 f _S)	MUTE	LOW	HIGH	LOW	LOW
		YES	PLL (128, 256, 384, 512 f _S)	PLL (64 f _S)	PLL (1 f _S)	DATA	DETECT	LOW	DATA	DATA
		NO	HOLD [‡] (128, 256, 384, 512 f _S)	HOLD [‡] (64 f _S)	HOLD [‡] (1 f _S)	MUTE	HOLD [‡]	HIGH	Unknown	HOLD [‡]
CRYSTAL	HIGH	After RESET	Crystal (128, 256, 384, 512 f _S)	Crystal (64 f _S)	Crystal (1 f _S)	MUTE	LOW	HIGH	LOW	LOW
		YES	Crystal (128, 256, 384, 512 f _S)	Crystal (64 f _S)	Crystal (1 f _S)	MUTE	DETECT	LOW	Unknown	LOW
		NO	Crystal (128, 256, 384, 512 f _S)	Crystal (64 f _S)	Crystal (1 f _S)	MUTE	Unknown	HIGH	Unknown	LOW

[†] In the PLL mode, the DIR1703 will be the same frequencies as the crystal mode after RESET; however, the frequency error is below 1%.

[‡] Holds the latest tracked frequency.

SCKO timing



SCKO Clock Pulse Width High t_{SCKH} 7 ns (min)
 SCKO Clock Pulse Width Low t_{SCKL} 7 ns (min)

[†] 1/128 f_S, 1/256 f_S, 1/384 f_S or 1/512 f_S.

bit rate detection

By using the SpAct frequency estimator (not the S/PDIF channel status bit), the DIR1703 automatically detects the sample rate of an incoming S/PDIF signal and indicates the frequency at the BRATE pins.

Table 6 lists the frequency ranges reported. Except for 88.2 and 96 kHz, these sample rates are the same as the channel status bit defined in the S/PDIF specifications. When the bit-rate is 88.2 or 96 kHz the indicator shows the same HL value. This state is not defined in the S/PDIF specifications.

Table 6. Incoming Sample Frequency Bits

SAMPLING RATE	BRATE1	BRATE0
32 kHz	HIGH	HIGH
44.1 kHz	LOW	LOW
48 kHz	LOW	HIGH
88.2 kHz	HIGH	LOW
96 kHz	HIGH	LOW

timing specification for PLL operation

lock-up time

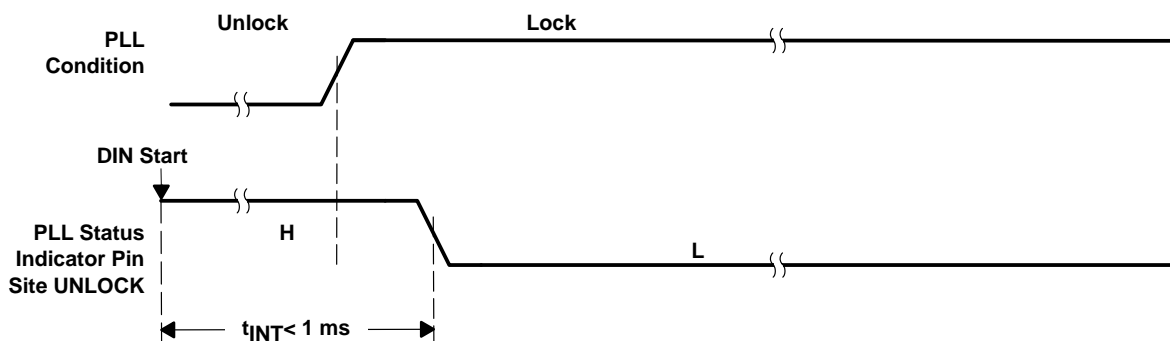


Figure 3. PLL Lock Up Timing

relation between audio-data-output timing and PLL condition indicator timing

In the PLL clock operation mode, when the S/PDIF signal is not detected after reset removal, audio clocks (SCKO, BCKO, LRCKO) which are not related to S/PDIF signal are generated by SpAct. The bit rate can be selected by setting pin BRSEL. If BRSEL is OPEN or connected to DGND, the default bit rate frequency is set to 48 kHz. If BRSEL is connected to one of the output pins BFRAME, EMFLG, URBIT, or CSBIT, the frequency is set to 32, 44.1, 88.2, or 96 kHz, respectively. Therefore, the initial frequency is the same as the crystal resonator, however, its error frequency is below 1% after reset.

When the analog PLL is still unlocked after at least ten rising-edges of the S/PDIF, a S/PDIF decoder can detect the incoming S/PDIF signal. Thus, DOUT becomes low (MUTE) until the analog PLL locks. This MUTE period is less than 1 ms (analog PLL’s lock-up time is less than 0.5 ms). When the decoder does not detect an incoming S/PDIF signal, UNLOCK will output high level status at the LRCKO clock transition. SCKO keeps its frequency at the latest tracked bit rate.

relation between audio-data-output timing and PLL condition indicator timing (continued)

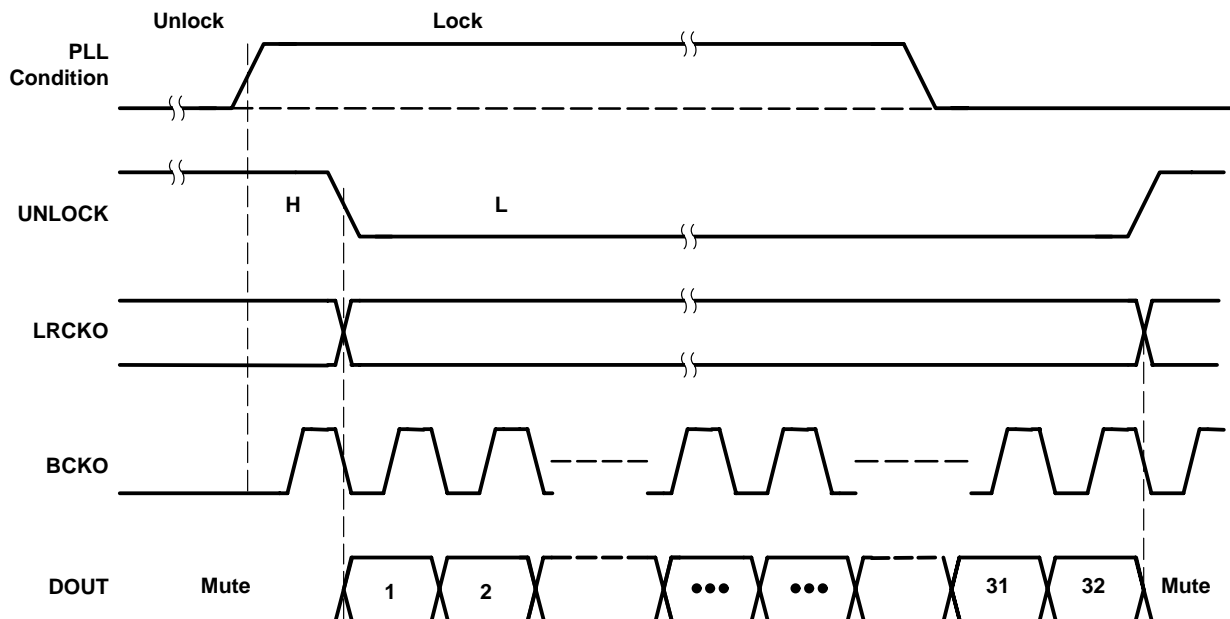


Figure 4. Relation Between Audio Data Output Timing and UNLOCK Flag Timing

unlock flag minimum pulse width time

CASE-A when PLL is unlocked

In the PLL clock operation mode, when PLL goes to unlock by a disconnected S/PDIF signal, the UNLOCK flag pin indicates high and the audio data output DOUT becomes low (MUTE). The MUTE period, $t_{(UNL)}$, is a minimum of 200 ms. In this period, SCKO, BCKO, and LRCKO frequencies hold the latest tracked frequency.

If the S/PDIF signal is connected again in this unlock period, the bit rate is changed to the incoming signal frequency, after at least 1 ms (before the UNLOCK flag becomes low). CKTRNS indicates the validity of SCKO. When CKTRNS is high, the frequency of SCKO, BCKO, and LRCKO is in transition.

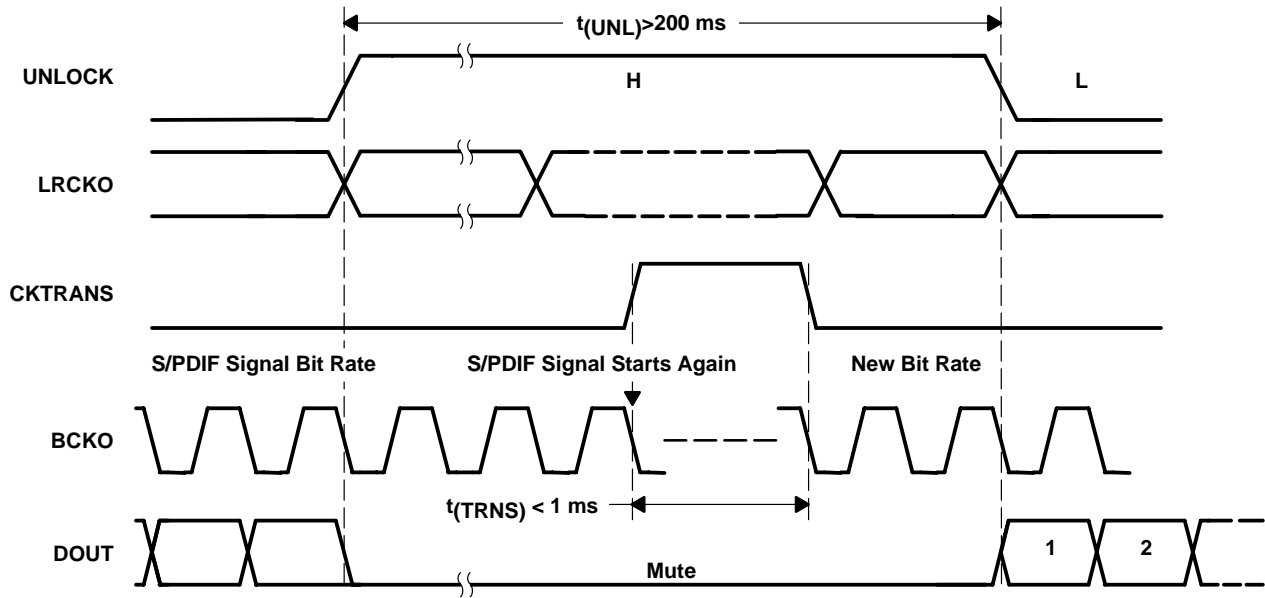


Figure 5. UNLOCK Flag Minimum Pulse Width Time for PLL Unlocked

CASE-B when parity error occurs

When a parity error occurs in one subframe interval, UNLOCK becomes high during this subframe, then returns low at the next arriving subframe.

During this subframe with parity error, the data output will hold the previous data of each channel.

CASE-B When Parity Error Occurs

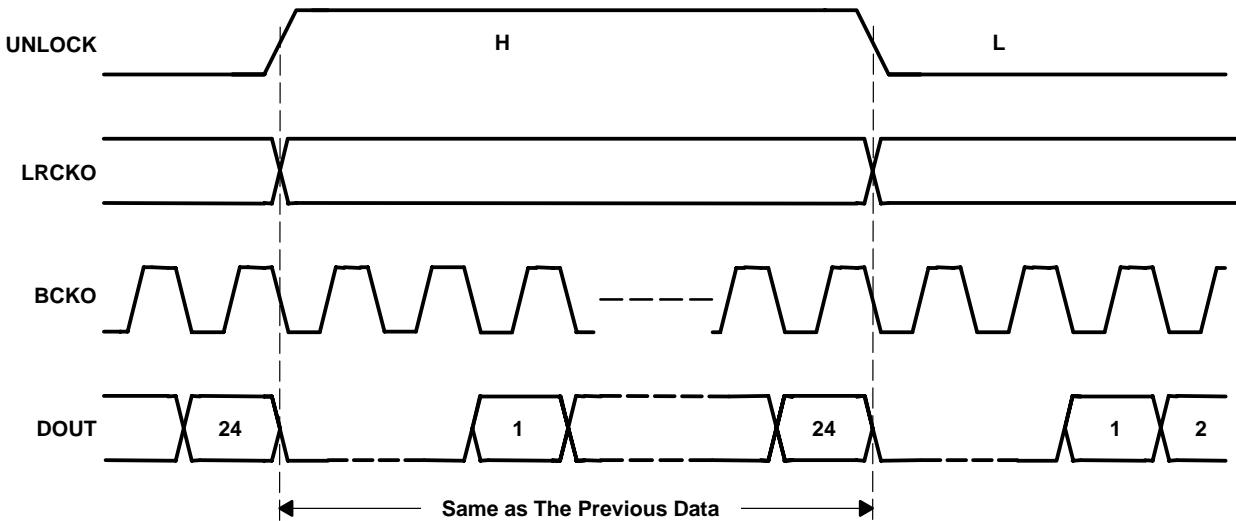


Figure 6. UNLOCK Timing for Parity Error

PCM audio interface

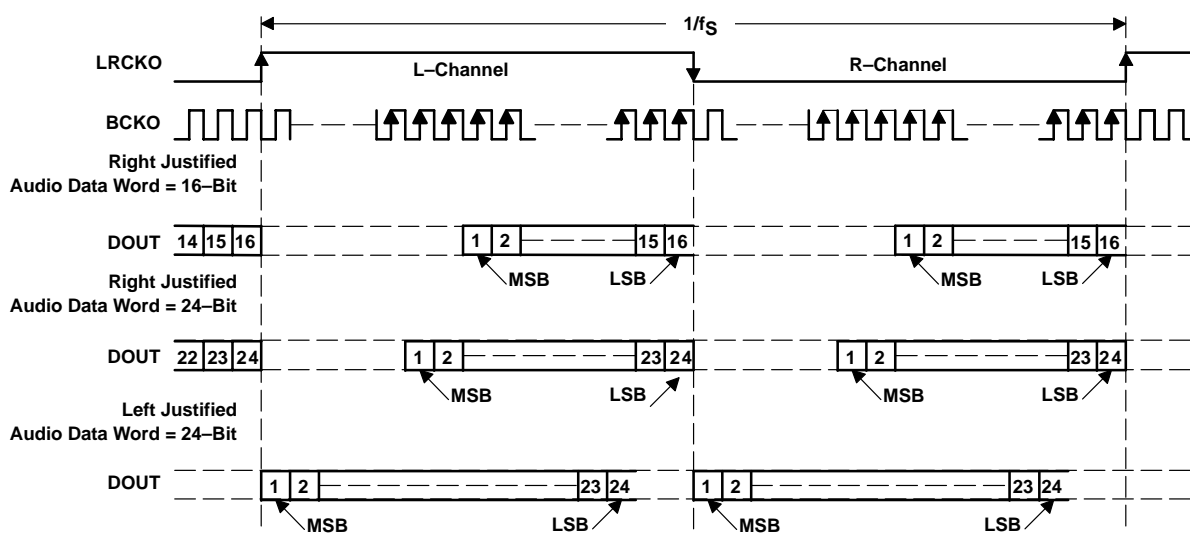
The DIR1703 can produce 16-bit or 24-bit output data in standard format and 24-bit output data in IIS format.

The PCM audio interface format of the DIR1703 is selected using the format pins FMT1, FMT0. Table 7 shows the FMT pin configuration.

Table 7. Audio Output Data Format Select

FMT1	FMT0	AUDIO DATA FORMAT
LOW	LOW	16 bit MSB first, Right justified
LOW	HIGH	24 bit MSB first, Right justified
HIGH	LOW	24 bit MSB first, Left justified
HIGH	HIGH	24 bit IIS

Standard Data Format; L-Channel = HIGH, R-Channel = LOW



IIS Data Format; L-Channel = LOW, R-Channel = HIGH

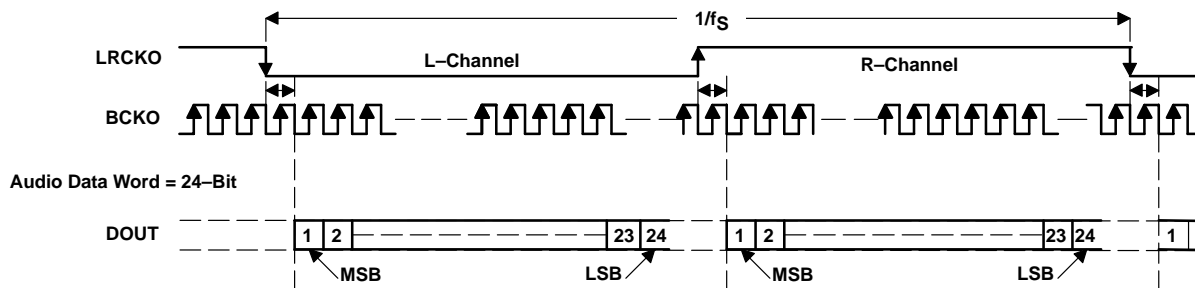
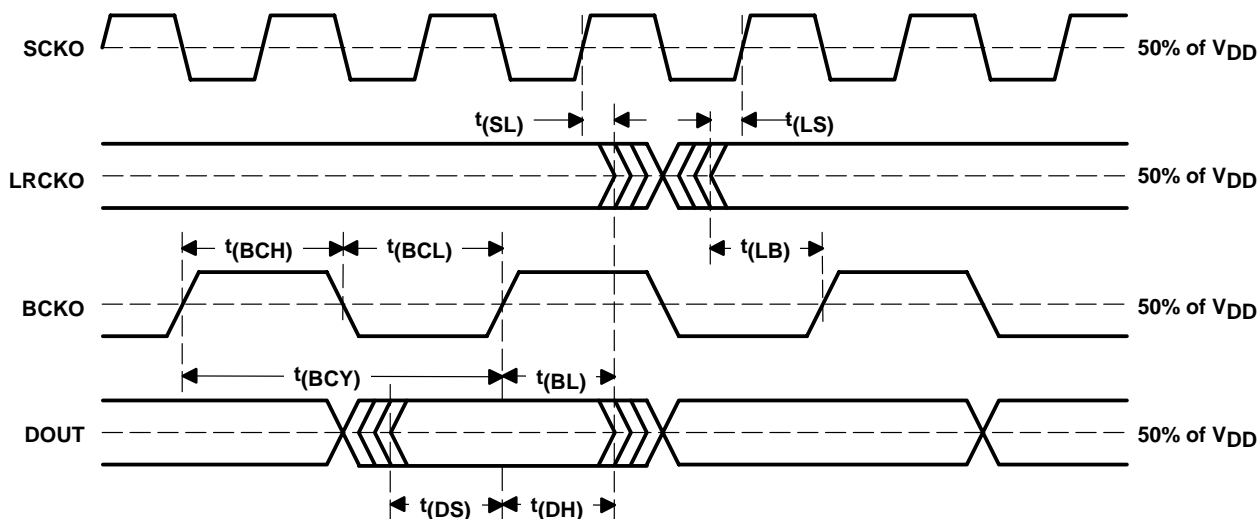


Figure 7. Audio Data Output Format

PCM audio interface (continued)



PARAMETERS		MIN	MAX	UNITS
$t(SL)$	SCKO rising edge to LRCKO edge	11		ns
$t(LS)$	LRCKO edge to SCKO rising edge	5		ns
$t(BCY)$	BCKO pulse cycle time		64 f_S	
$t(BCL)$	BCKO pulse width low	78		ns
$t(BCH)$	BCKO pulse width high	78		ns
$t(BL)$	BCKO rising edge to LRCKO edge	78		ns
$t(LB)$	LRCKO edge to BCKO rising edge	78		ns
$t(DS)$	DOUT setup time	78		ns
$t(DH)$	DOUT hold time	78		ns

Figure 8. Audio Data Output Timing

dedicated output pins for both professional and consumer applications

The DIR1703 has parallel output pins for both professional and consumer applications. In the professional mode de-emphasis flag EMFLG indicates a 50/15- μ s time constant pre-emphasis. Professional mode is set when Bit 0 of CSBIT Byte 0 is high. When Bits 2 to 4 of CSBIT Byte 0 is 110, the EMFLG becomes high. In other cases, EMFLG is low. Audio/non-audio flag ADFLG indicates S/PDIF data mode, i.e., Bit 1 of CSBIT Byte 0. When ADFLG is low, S/PDIF data includes PCM audio signal. In other cases, ADFLG is high.

In the consumer mode EMFLG indicates 2-channel audio with a 50/15- μ s time constant pre-emphasis. Consumer mode is set when Bit 0 of CSBIT Byte 0 is low. When Bits 3 to 5 of CSBIT Byte 0 is 100, EMFLG becomes high. In other cases, EMFLG is low. The ADFLG signal indicates whether S/PDIF includes digital data, such as AC-3 or not. When Bit 1 of CSBIT Byte 0 is high, the incoming S/PDIF includes a non-audio signal. In other cases, ADFLG is low.

These dedicated output pins are checked for only L-ch CS information. The DIR1703 does not support CRC check function in the professional mode. As for other flags, CS bit and user-bit for professional and consumer applications, are directly supplied by serial mode at CSBIT (pin 15) and URBIT (pin 16). These pins indicate L-ch and R-ch information sequentially.

dedicated output pins for both professional and consumer applications (continued)

Audio data and clock timing are described below. The serial output data starts after 16 ± 8 BCKO clocks from when the corresponding subframe arrives. When B subframe arrives, the BFRAME pin becomes high during $1/f_S \times 32$ (s), then BFRAME returns to low after 32 frames.

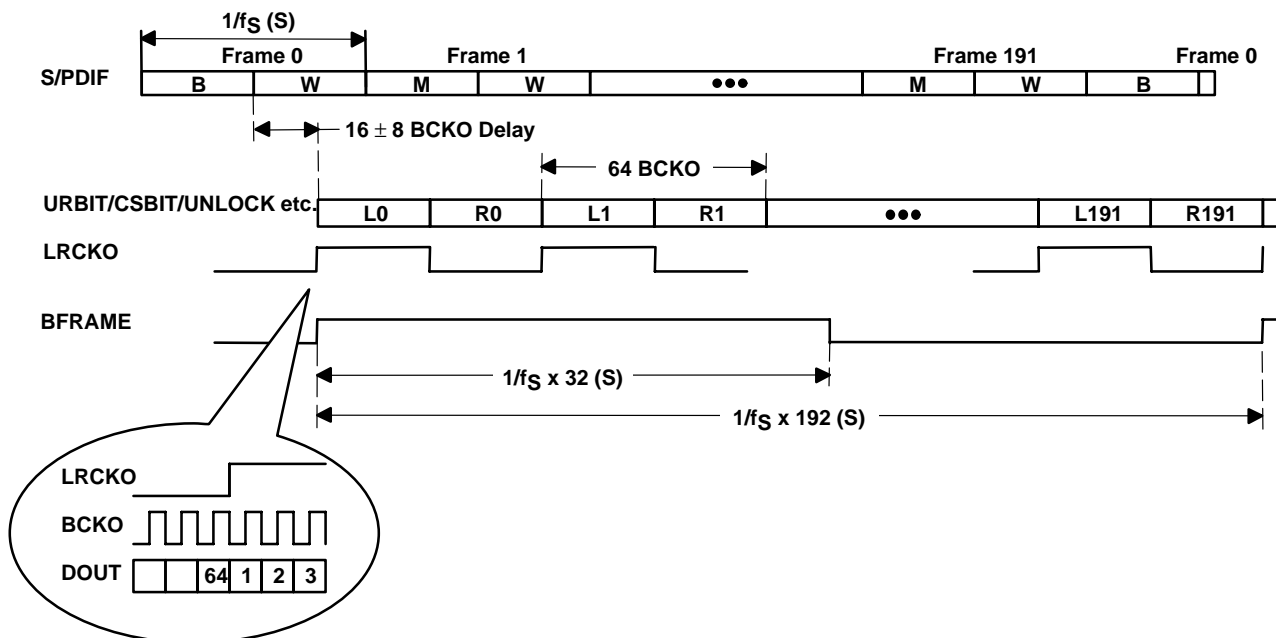
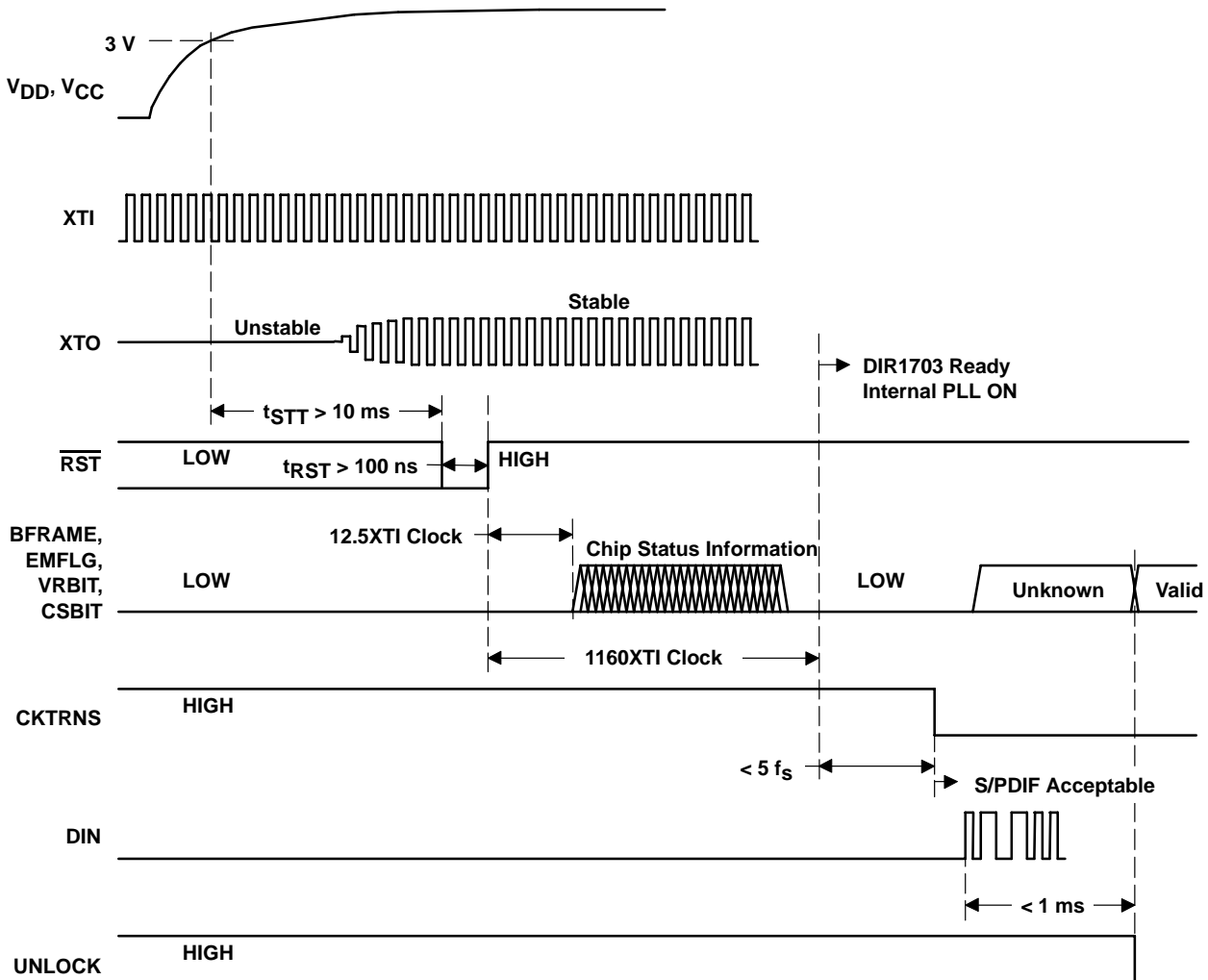


Figure 9. Timing Chart for Audio Data and Channel Status

reset sequence

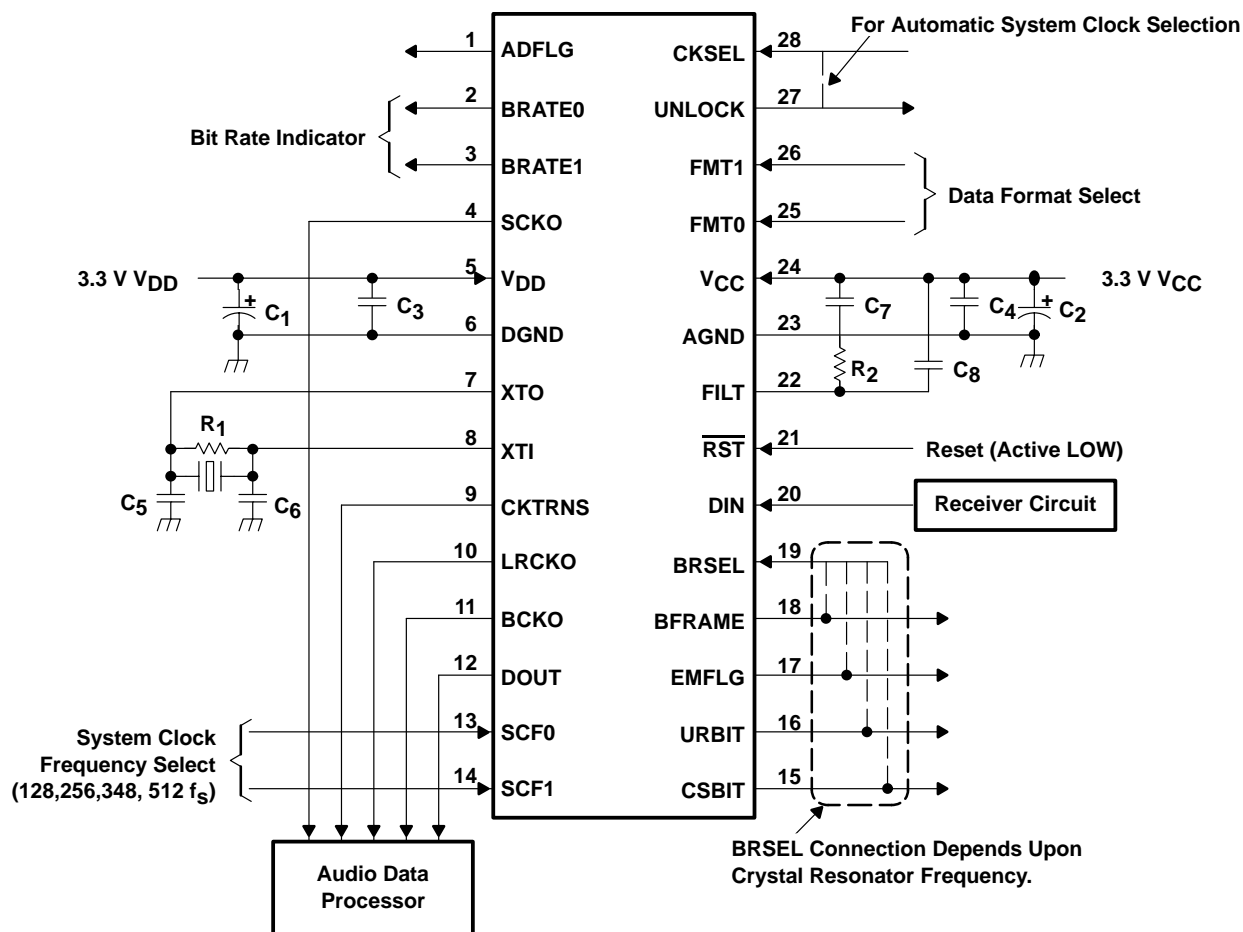
The DIR1703 requires external reset operation after power on. Figure 10 shows the reset sequence after power on. The DIR1703 is ready for receiving S/PDIF signal when the internal reset sequence has finished and CKTRNS goes to LOW. BFRAME, EMFLG, URBIT and CSBIT pins are used for configuration during the period from the rising edge of $\overline{\text{RST}}$ to the falling edge of CKTRNS. S/PDIF signal is accepted after CKTRNS goes to LOW. The minimum pulse width of $\overline{\text{RST}}$, t_{RST} is 100 ns. The $\overline{\text{RST}}$ delay after the power supply reaches 3 V should be at least 10 ms. All of the output pins except CKTRNS and UNLOCK are LOW during $\overline{\text{RST}}$ LOW.



NOTE: SCF0 and SCF1 should be settled during $\overline{\text{RST}}$ assertion. The change of SCF0 and SCF1 is not permitted during normal operation. When the change is needed, the reset sequence must be started by asserting $\overline{\text{RST}}$ again.

Figure 10. After Power ON

typical circuit connection

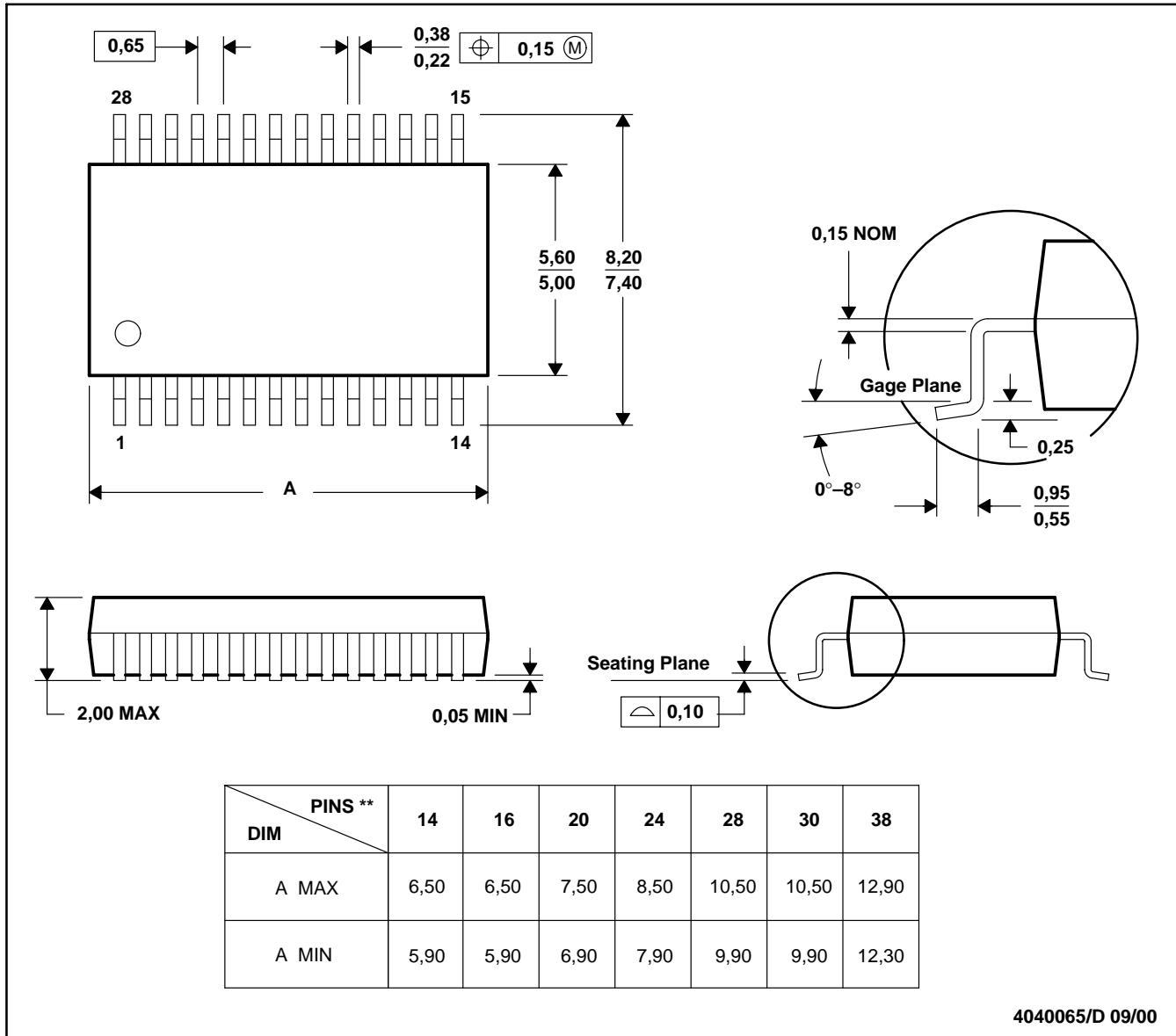


- C₁, C₂: Bypass Capacitor, 1 μ F to 10 μ F
 C₃, C₄: Bypass Capacitor, 0.01 μ F to 0.1 μ F
 C₅, C₆: OSC Capacitor, 10 to 33 pF
 C₇: Loop Filter Capacitor, 0.068 μ F
 C₈: Loop Filter Capacitor, 0.0082 μ F
 R₁: OSC Resistor, 1 M Ω
 R₂: Loop Filter Resistor, 1.2 k Ω

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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